In the Specification:

Please replace paragraph [00022] beginning on page 6 with the following rewritten paragraph:

[00022] When an interrupt is loaded in the register ~~INT PENDIG REG~~ INT. PENDING REG. the corresponding counter previously loaded with the value stored in the corresponding PRIORITY REGISTER is enabled to be periodically incremented by the respective increment signal of the signals fed to the counters block ~~PRIORITY TRIGGERS~~ PRIORITY COUNTERS. The circuit IRQ MASK AND PRIORITY LOGIC reads from the periodically incremented counters the priority values, identifies which of the pending interrupts has the highest priority, generates an interrupt request IRQ REQ that is sent to the state machine IRQ SM and an internal signal HIGHEST PRIORITY INT representing the priority of the interrupt INTn that must be served.